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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/583,201	05/30/2000	Kendall F. Tidwell	10992479-1	1466

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EXAMINER	
MONESTIME, MACKLY	
ART UNIT	**PAPER NUMBER**
2676	

DATE MAILED: 12/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/583,201	TIDWELL ET AL.	
	Examiner	Art Unit	
	Mackly Monestime	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Response to Amendment

1. The amendment received on October 30, 2003 has entered and carefully considered. Claims 1-23 are still pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al (US Patent No. 5,924,111) in view of Hannah (US Patent No. 5,038,297).

4. Hannah et al was cited in the last office action.

5. As per claims 1-2, 6 and 11-12, Huang et al substantially disclosed the invention as claimed including a system for clearing data residing in a memory region, comprising: a controller (Fig. 5, Item No. 132); and a memory coupled to said controller having said memory region subdivided into a plurality of sub-regions (Fig. 5, Item No. 134), each said sub-region comprising a plurality of storage elements (col. 6, lines 40-49; col. 16, lines 11-14).

Huang et al did not explicitly disclose that the controller is designed to write clear data concurrently to each one of said plurality of sub-region; but Huang et al did disclosed that the

memory controller receives instructions to read pixel data from, and write pixel data into, the frame buffer, and further translate the address of the pixel data and output appropriate control and address signals to the frame buffer for accessing the desired pixel data (col. 8, lines 31-38). However, Hannah disclosed a graphics update controller being able to write simultaneously clear data into a plurality of VRAM chips in the frame buffer (col. 4, lines 18-20, lines 45-49; col. 5, lines 1-4, lines 28-30; col. 10, lines 62-67) . It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have utilized the controller taught by Hannah into the system of Huang et al because doing so would provide an efficient method for clearing of a region of the screen by writing a plurality of bits into a plurality of pixel locations in the frame buffer.

6. As per claim 3, Huang et al disclosed that the memory region is subdivided into consecutive and adjacent sub-regions (col. 14, lines 11-15).

7. As per claims 4-5, Huang et al disclosed that the memory region is subdivided into sub-regions of equal dimensions and of different dimensions (col. 4, lines 1-2; col. 8, lines 64-67; col. 9, lines 1-3).

8. As per claim 7, Huang et disclosed that the memory is a frame buffer associated with a graphics display (Fig. 5, Items No. 130, 134).

9. As per claim 8, Huang et al disclosed that the controller is a frame buffer controller (Fig. 5, Item No. 132).

10. As per claim 9, Huang et al did not explicitly disclose that the plurality of sub-regions are individually identified by location in said memory by a pointer register. However, as is known well known in the memory art, pointers are used to identify or to indicate location of an item of data, in computer graphics, a pointer may be used to conduct interactive graphic operations such as selection of one member of a predetermined set of display elements, or indication of a position on a display space. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized a pointer register into the teachings of Huang et al because doing would facilitate the easy identification of the type of the data in the memory so that such data can be easily accessed in order to draw the relevant portion of an image within the respective location in the frame buffer; thereby enhance the efficiency of the system.

11. As per claim 10, Huang et al further disclosed a processor configured to determine the location of said memory region (Fig. 5, Item No. 112).

12. Claims 13-17, 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al in view of Hannah as applied to claims 1-12 above, and in further in view of Maeda (US Patent No. 6,067,382).

13. Maeda was cited in the last office action.

14. As per claims 13-14, Huang et al and Hannah did not disclosed the steps of: a processor to determine dimension and a position of at least one image on said graphic display device, wherein said at least one image is to be cleared. However, Maeda disclosed a processor to determine dimension and a position of at least one image on said graphic display device, wherein

said at least one image is to be cleared (col. 24, lines 34-35; col. 29, lines 10-15; lines 23-40 and col. 32, lines 58-65). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the cited references because doing so would provide a system being able to identify the position and the location of the data within the sub-regions so that such data may be appropriately processed by the graphics system.

15. As per claims 15-17, 19-20 and 21, Huang et al substantially disclosed the invention as claimed including a system for clearing data residing in a memory region, comprising: a controller (Fig. 5, Item No. 132); and a memory coupled to said controller having said memory region subdivided into a plurality of sub-regions (Fig. 5, Item No. 134), each said sub-region comprising a plurality of storage elements (col. 6, lines 40-49; col. 16, lines 11-14).

Huang et al did not explicitly disclose that the controller is designed to write clear data concurrently to each one of said plurality of sub-region; but Huang et al did disclosed that the memory controller receives instructions to read pixel data from, and write pixel data into, the frame buffer, and further translate the address of the pixel data and output appropriate control and address signals to the frame buffer for accessing the desired pixel data (col. 8, lines 31-38). However, Hannah disclosed a graphics update controller being able to write simultaneously clear data into a plurality of VRAM chips in the frame buffer (col. 4, lines 18-20, lines 45-49; col. 5, lines 1-4, lines 28-30; col. 10, lines 62-67) . It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have utilized the controller taught by Hannah into the system of Huang et al because doing so would provide an efficient method for clearing of

a region of the screen by writing a plurality of bits into a plurality of pixel locations in the frame buffer.

The combination did not disclosed the steps of: a processor to determine dimension and a position of at least one image on said graphic display device, wherein said at least one image is to be cleared. However, Maeda disclosed a processor to determine dimension and a position of at least one image on said graphic display device, wherein said at least one image is to be cleared (col. 24, lines 34-35; col. 29, lines 10-15; lines 23-40 and col. 32, lines 58-65). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the cited references because doing so would provide a system being able to identify the position and the location of the data within the sub-regions so that such data may be appropriately processed by the graphics system.

16. Claims 18 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al in view of Hannah and Maeda as applied to claims 15-17 and 21 above, and in further in view of Deering et al (US Patent No. 5,544,306).

17. Deering et al was cited in the last office action.

18. As per claims 18 and 22; the combination did not disclose the steps of associating a plurality of location identifiers wherein one location is associated with each one of said plurality of subregions residing in said frame buffer and writing clear data begins at said plurality of sub-region identified by said plurality of location identifiers. However, Deering et al disclosed a plurality of dirty tags associated to a plurality of DRAM banks; and a rendering controller

employs color expansion and writes common color value to many pixels in the DRAM banks A-D (col. 19, lines 6-25; col. 20, lines 55-67; col. 21, lines 1-6). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the cited references because doing so would provide a system being able to identify the data within the sub-regions so that such data may be appropriately processed by the graphics system.

19. As per claim 23, the combination did not disclosed the steps of: a processor to determine dimension and a position of at least one image on said graphic display device, wherein said at least one image is to be cleared. However, Maeda disclosed a processor to determine dimension and a position of at least one image on said graphic display device, wherein said at least one image is to be cleared (col. 24, lines 34-35; col. 29, lines 10-15; lines 23-40 and col. 32, lines 58-65). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the cited references because doing so would provide a system being able to identify the position and the location of the data within the sub-regions so that such data may be appropriately processed by the graphics system.

Response to Arguments

20. Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

21. Applicant is required to give full consideration to these prior art references when responding to this office action.

The prior arts made of record and not relied upon is considered pertinent to applicant's disclosure.

Nishida (US Patent No. 6,560,686) taught a memory device with variable bank partition architecture.

Kishida (US Patent No. 6,170,039) taught a memory controller for interchanging memory against memory error in interleave memory system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mackly Monestime whose telephone number is (703) 305-3855. The examiner can normally be reached on Monday to Thursday from 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bella Matthew, can be reached on (703) 308-6829.

Any response to this action should be mailed to:

Commissioner of Patent and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, Va, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Mackly Monestime

Patent Examiner

December 2, 2003

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600